



2123/ IAW

Patent

Docket No.: CYPR-CD01208

Information Disclosure Statement Transmittal

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Date of Deposit:	10/17/05	Name of Person Making the Deposit:	KATHERINE RINALDI
		Signature of the Person Making the Deposit:	<i>Katherine Rinaldi</i>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Craig Nemecek

Application No.: 09/989,777

Group Art Unit:

Filed: 11/19/01

Examiner:

Title: SLEEP AND STALL IN AN IN-CIRCUIT EMULATION SYSTEM

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

- ☒ Information Disclosure statement and late filing fee of \$180.00
☒ Form 1449
☒ Other: REFERENCE

Fee Calculation (for other than a small entity)				
Fee Items			Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere)			\$.00	\$0.00
Information Disclosure Statement, late filing			\$180.00	\$180.00
Other:				\$0.00
Total Fees				\$180.00

PAYMENT OF FEES

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 - ☐ Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

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Respectfully submitted,

Date: _____

10/17/05

By: _____



Kevin A. Brown

Reg. No. 56,303



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD01208.....

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Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
6,144,327	PROGRAMMABLE INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
6,016,554	METHOD FOR EVENT-RELATED FUNCTIONAL TESTING OF A MICROPROCESSOR	01/18/00
5,978,584	DEBUGGING APPARATUS FOR DEBUGGING A PROGRAM BY CHANGING HARDWARE ENVIRONMENTS WITHOUT CHANGING PROGRAM OPERATION STATE	11/02/99
6,356,862	HARDWARE AND SOFTWARE CO-VERIFICATION EMPLOYING DEFERRED SYNCHRONIZATION	03/12/02
6,058,263	INTERFACE HARDWARE DESIGN USING INTERNAL AND EXTERNAL INTERFACES	05/02/00
5,999,725	METHOD AND APPARATUS TRACING A NODE OF AN EMULATION	12/07/99
6,289,300	INTEGRATED CIRCUIT WITH EMBEDDED EMULATOR AND EMULATION SYSTEM FOR USE WITH SUCH AN INTEGRATED CIRCUIT	09/11/01
6,366,878	CIRCUIT ARRANGEMENT FOR IN-CIRCUIT EMULATION OF A MICROCONTROLLER	04/02/02
6,298,320	SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE	10/02/01
5,889,988	DEBUGGER FOR DEBUGGING TASKS IN AN OPERATING SYSTEM WITH VIRTUAL DEVICES DRIVER	03/30/99
6,487,700	SEMICONDUCTOR DEVICE SIMULATING APPARATUS AND SEMI-CONDUCTOR TEST PROGRAM DEBUGGING APPARATUS USING IT	11/26/02

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5,559,996	LEVEL CONVERTER INCLUDING WAVE-SHAPING CIRCUIT AND EMULATOR MICROCOMPUTER INCORPORATING THE LEVEL CONVERTER	09/24/96
6,223,272	TEST VECTOR VERIFICATION SYSTEM	04/24/01
5,964,893	DATA PROCESSING SYSTEM FOR PERFORMING A TRACE FUNCTION AND METHOD THEREFOR	10/12/99
6,107,826	INTERCONNECT STRUCTURE FOR FPGA WITH CONFIGURABLE DELAY LOCKED LOOP	08/22/00
6,032,268	PROCESSOR CONDITION SENSING CIRCUITS, SYSTEMS AND METHODS	02/29/00
5,805,792	EMULATION DEVICES, SYSTEMS, AND METHODS	09/08/98
5,590,354	MICROCONTROLLER PROVIDED WITH HARDWARE FOR SUPPORTING DEBUGGING AS BASED ON BOUNDARY SCAN STANDARD TYPE EXTENSIONS	12/31/96
6,161,199	NON-INTRUSIVE IN-SYSTEM DEBUGGING FOR A MICROCONTROLLER WITH IN-SYSTEM PROGRAMMING CAPABILITIES USING IN-SYSTEM DEBUGGING CIRCUITRY AND PROGRAM EMBEDDED IN-SYSTEM DEBUGGING COMMANDS	12/12/00
6,564,179	DSP EMULATING A MICROCONTROLLER	05/13/03
5,587,957	CIRCUIT FOR SHARING A MEMORY OF A MICROCONTROLLER WITH AN EXTERNAL DEVICE	12/24/96
6,385,742	MICROPROCESSOR DEBUGGING MECHANISM EMPLOYING SCAN INTERFACE	05/07/02
5,546,562	METHOD AND APPARATUS TO EMULATE VLSI CIRCUITS WITHIN A LOGIC SIMULATOR	08/13/96
6,718,294	SYSTEM AND METHOD FOR SYNCHRONIZED CONTROL OF SYSTEM SIMULATORS WITH MULTIPLE PROCESSOR CORES	04/06/04
5,371,878	SYSTEM FOR ANALYSIS OF EMBEDDED COMPUTER SYSTEMS	12/06/94
5,321,828	HIGH SPEED MICROCOMPUTER IN-CIRCUIT EMULATOR	06/14/94
5,752,013	METHOD AND APPARATUS FOR PROVIDING PRECISE FAULT TRACING IN A SUPERSCALAR MICROPROCESSOR	05/12/98
6,374,370	METHOD AND SYSTEM FOR FLEXIBLE CONTROL OF BIST REGISTERS BASED UPON ON CHIP EVENTS	04/16/02
5,630,052	SYSTEM DEVELOPMENT AND DEBUG TOOLS FOR POWER MANAGEMENT FUNCTIONS IN A COMPUTER SYSTEM	05/13/97
6,075,941	MICROCOMPUTER	06/13/00
5,325,512	CIRCUIT EMULATOR	06/28/94
6,094,730	HARDWARE-ASSISTED FIRMWARE TRACING METHOD AND APPARATUS	07/25/00
6,829,727	IN-CIRCUIT EMULATION OF SINGLE CHIP MICROCONTROLLERS	12/07/04
5,663,900	ELECTRONIC SIMULATION AND EMULATION SYSTEM	09/02/97
6,347,395	METHOD AND ARRANGEMENT FOR RAPID SILICON PROTOTYPING	02/12/02
6,009,270	TRACE SYNCHRONIZATION IN A PROCESSOR	12/28/99
6,185,522	METHOD AND SYSTEM FOR EMULATING MICROCONTROLLERS	02/06/01
6,223,144	METHOD AND APPARATUS FOR EVALUATING SOFTWARE PROGRAMS FOR SEMICONDUCTOR CIRCUITS	04/24/01
6,173,419	FIELD PROGRAMMABLE GATE ARRAY FPGA EMULATOR FOR DEBUGGING SOFTWARE	01/09/01
6,516,428	ON-CHIP DEBUG SYSTEM	02/04/03
6,581,191	HARDWARE DEBUGGING IN A HARDWARE DESCRIPTION LANGUAGE	06/17/03
5,630,102	IN-CIRCUIT-EMULATION EVENT MANAGEMENT SYSTEM	05/13/97
6,810,442	MEMORY MAPPING SYSTEM AND METHOD	10/26/04
5,574,892	USE OF BETWEEN-INSTRUCTION BREAKS TO IMPLEMENT COMPLEX IN-CIRCUIT EMULATION FEATURES	11/12/96
5,331,571	TESTING AND EMULATION OF INTEGRATED CIRCUITS	07/19/94
5,911,059	METHOD AND APPARATUS FOR TESTING SOFTWARE	06/08/99
5,572,665	SEMICONDUCTOR INTEGRATED CIRCUIT FOR DEVELOPING A SYSTEM USING A MICROPROCESSOR	11/05/96
5,127,103	REAL-TIME TRACING OF DYNAMIC LOCAL DATA IN HIGH LEVEL LANGUAGES IN THE PRESENCE OF PROCESS CONTEXT SWITCHES	06/30/92
6,618,854	REMOTELY ACCESSIBLE INTEGRATED DEBUG ENVIRONMENT	09/09/03

5,748,875	DIGITAL LOGIC SIMULATION/EMULATION SYSTEM	05/05/98
6,202,044	CONCURRENT HARDWARE-SOFTWARE CO-SIMULATION	03/13/01
5,493,723	PROCESSOR WITHIN-SYSTEM EMULATION CIRCUITRY WHICH USES THE SAME GROUP OF TERMINALS TO OUTPUT PROGRAM COUNTER BITS	02/20/96

The Examiner's attention is respectfully directed to the following U.S. Published Patent Applications:

<u>Pub. No.</u>	<u>Pub. Title</u>	<u>Pub. Date</u>
2002/0052729	APPARATUS AND METHOD FOR VERIFYING A LOGIC FUNCTION OF A SEMICONDUCTOR CHIP	05/02/02
2003/0149961	APPARATUS, METHOD, AND PROGRAM FOR BREAKPOINT SETTING	08/07/03
2003/0056071	ADAPTABLE BOOT LOADER	03/20/03
2002/0156885	PROTOCOL EMULATOR	10/24/02
2002/0116168	METHOD AND SYSTEM FOR DESIGN VERIFICATION OF ELECTRONIC CIRCUITS	08/22/02

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

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Respectfully submitted,

Date: 10/17/05

By: 
 Kevin A. Brown
 Reg. No. 56,303



Attorney Docket No.: CYPR-CD01208

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Craig Nemecek

Application No.: 09/989,777

Group Art Unit:

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Examiner:

Title: SLEEP AND STALL IN AN IN-CIRCUIT EMULATION SYSTEM

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
	C	6,016,554	01/18/00	Skrovan et al.	741	25	07/28/97
	D	5,978,584	11/02/99	Nishibata et al.	395	704	06/19/97
	E	6,356,862	03/12/02	Bailey	703	16	09/24/98
	F	6,058,263	05/02/00	Voth	395	500.46	06/03/96
	G	5,999,725	12/07/99	Barbier et al.	395	500.49	04/17/98
	H	6,289,300	09/11/01	Brannick et al.	703	28	02/06/98
	I	6,298,320	10/02/01	Buckmaster et al	703	28	02/17/98
	J	6,366,878	04/02/02	Grunert	703	28	09/28/98
	K	5,889,988	03/30/99	Held	395	673	11/08/96
	L	6,487,700	11/26/02	Fukushima	716	4	03/08/00
	M	5,559,996	09/24/96	Fujioka	395	500	01/11/94
	N	6,223,272	04/24/01	Coehlo et al.	712	1	07/15/98
	O	5,964,893	10/12/99	Circello et al.	714	39	08/30/95
	P	6,107,826	08/22/00	Young et al.	326	41	08/19/98
	Q	6,302,268	02/29/00	Swoboda et al.	714	30	02/04/92
	R	5,805,792	09/08/98	Swoboda et al.	395	183.04	03/21/97
	S	5,590,354	12/31/96	Klapproth et al.	395	800	07/28/94
	T	6,161,199	12/12/00	Szeto et al.	714	30	12/12/97
	U	6,564,179	05/13/03	Belhaj	703	26	07/26/99
	V	5,587,957	12/24/96	Kowalczyk et al.	365	230.03	09/29/95
	W	6,385,742	05/07/02	Kirsh et al.	714	39	03/05/99
	X	5,546,562	08/13/96	Patel	395	500	08/13/96
	Y	6,718,294	04/06/04	Bortfeld	703	20	05/16/00
	Z	5,371,878	12/06/94	Coker	395	500	09/09/93
	AA	5,321,828	06/14/94	Phillips et al.	395	500	06/07/91
	BB	5,752,013	05/12/98	Christensen et al.	395	568	06/30/93
	CC	6,374,370	04/16/02	Bockhaus et al.	714	39	10/30/98
	DD	5,630,052	05/13/97	Shah	395	183.14	10/18/96
	EE	6,075,941	06/13/00	Itoh et al.	395	704	01/22/98
	FF	5,325,512	06/28/94	Takahashi	395	500	07/12/93
	GG	6,094,730	07/25/00	Lopez et al.	714	28	10/27/97
	HH	6,829,727	12/07/04	Pawloski	714	28	01/12/01

	II	5,663,900	09/02/97	Bhandari et al.	364	578	05/09/95
	JJ	6,347,395	02/12/02	Payne et al.	716	18	12/18/98
	KK	6,009,270	12/28/99	Mann	395	704	12/07/97
	LL	6,185,522	02/06/01	Bakker	703	28	05/18/98
	MM	6,223,144	04/24/01	Barnett et al.	703	22	03/24/98
	NN	6,173,419	01/09/01	Barnett	714	28	05/14/98
	OO	6,516,428	02/04/03	Wenzel et al.	714	28	01/22/99
	PP	6,581,191	06/17/03	Schubert et al.	716	4	11/28/00
	QQ	5,630,102	05/13/97	Johnson et al.	395	500	12/19/94
	RR	6,810,442	10/26/04	Lin et al.	710	22	09/12/01
	SS	5,574,892	11/12/96	Christensen	395	500	02/28/95
	TT	5,331,571	07/19/94	Aronoff et al.	364	490	07/22/92
	UU	5,911,059	06/08/99	Profit, Jr.	395	500	12/18/96
	VV	5,572,665	11/05/96	Nakabayashi	395	183.04	11/01/95
	WW	5,127,103	06/30/92	Hill et al.	395	575	11/16/90
	XX	6,618,854	09/09/03	Mann	717	124	02/18/97
	YY	5,748,875	05/05/98	Tzori	395	183.05	06/12/96
	ZZ	6,202,044	03/13/01	Tzori	703	28	06/12/98
	AAA	5,493,723	02/20/96	Beck et al.	395	500	10/27/94

U.S. Published Patent Application

Examiner Initial	No.	Pub. No.	Pub. Date	Patentee	Class	Sub-class	Filing Date
	BBB	2002/0156885	10/24/02	Thakkar	709	224	04/23/01
	CCC	2002/0116168	08/22/02	Kim	703	28	11/15/99
	DDD	2003/0056071	03/20/03	Triece et al.	711	165	09/18/01
	EEE	2003/0149961	08/07/03	Kawai et al.	717	129	02/05/03
	FFF	2002/0052729	05/02/02	Kyung et al.	703	28	01/17/01

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	GGG	Dahl et al., "EMULATION OF THE SPARCLE MICROPROCESSOR WITH THE MIT VIRTUAL WIRES EMULATION SYSTEM"; 1994; IEEE; pages 14-22
	HHH	Bauer et al.; "A RECONFIGURABLE LOGIC MACHINE FOR FAST EVENT-DRIVEN SIMULATION"; 1998; Design Automation Conference Proceedings; pages 668-671
	III	Bursky; "FPGA COMBINES MULTIPLE INTERFACES AND LOGIC"; Electronic Design; Vol. 48 No. 20; pp 74-78 (Oct. 2, 2000)
	JJJ	Anonymous, "WARP NINE ENGINEERING – THE IEEE 1284 EXPERTS-F/PORT PRODUCT SHEET"; undated web page found at http://www.fapo.com/fport.htm
	KKK	Anonymous; "F/PORT: FAST PARALLELL PORT FOR THE PC: INSTALLATION MANUAL : Release 7.1," circa 1997, available for download from http://www.fapo.com/fport.htm
	LLL	Nam et al. ; "FAST DEVELOPMENT OF SOURCE-LEVEL DEBUGGING SYSTEM USING HARDWARE EMULATION"; IEEE 2000; pages 40-404
	MMM	Huang et al.; "ICEBERG: AN EMBEDDED IN-CIRCUIT EMULATOR SYNTHESIZER FOR MICROCONTROLLERS"; ACM 1999; pages 580-585
	NNN	Khan et al.; "FPGA ARCHITECTURES FOR ASIC HARDWARE EMULATORS"; IEEE 1993; pages 336-340
	OOO	Oh et al.; "EMULATOR ENVIRONMENT BASED ON AN FPGA PROTOTYPING BOARD"; IEEE 21-23; June 2000; pages 72-77
	PPP	Hong et al.; "AN FPGA-BASED HARDWARE EMULATOR FOR FAST FAULT EMULATION"; IEEE 1997; pages 345-348
	QQQ	Ching et al.; "AN IN-CIRCUIT EMULATOR FOR TMS320C25"; IEEE 1994; pages 51-56
	RRR	Pasternak; "IN-CIRCUIT-EMULATION IN ASIC ARCHITECTURE CORE DESIGNS"; IEEE 1989' pages P6-4.1-P6-4.4
	SSS	Melear; "USING BACKROUND MODES FOR TESTING, DEBUGGING AND EMULATION OF MICROCONTROLLERS"; IEEE 1997; pages 90-97
	TTT	Walters; "COMPUTER-AIDED PROTOTYPING FOR ASIC-BASED SYSTEMS"; 1991; IEEE Design & Test of Computers
	UUU	Anonymous; "JEEN™ JTAG EMBEDDED ICE ETHERNET INTERFACE"; August 1999; Embedded Performance, Inc.; 3 pages
	VVV	Sedory; "A GUIDE TO DEBUG"; 2004' retrieved on 5/20/05
	WWW	"MICROSOFT FILES SUMMARY JUDGEMENT MOTIONS"; February 1999; Microsoft PressPass; retrieved on 5/20/05 from http://www.microsoft.com/presspass/press/1999/feb99/Feb99/Calderapr.asp ; pages 1-6
	XXX	Anonymous; "USING DEBUG"; 1999; Prentice-Hall Publishing; pages 1-20
	YYY	XEROX; MESA DEBUGGER DOCUMENTATION "; April 1979; XEROX Systems Development Department; Version 5.0; pages 1-30
	ZZZ	Stallman et al.; "DEBUGGING WITH THR GNU SOURCE-LEVEL DEBUGGER"; January 1994; retrieved on May 2, 2005 from http://www.cs.utah.edu ; Stopping and Continuing"
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.